DALSA

DALSA IL-P1-xxxx-B Image Sensors

The IL-P1-xxxx-B sets new line scan standards. Its unprecedented design and fabrication sophistication has produced superior performance: high blue response and low image lag, two taps for high line rates, low-voltage clocks—and DALSA's standard 100% fill factor.

■ Highly sensitive, with responsivity reaching $12V/(\mu J/cm^2)$

Features

■ 2 taps @ 25MHz data rate per tap
■ Line rates to 87kHz
■ Low voltage clocks (<5V)
■ 10µm (H) x 10µm (V) pixels, 100% fill factor
■ 512, 1024, or 2048 pixels
■ Antiblooming and exposure control

Description

Physical Characteristics	IL-P1-xxxx-B
Pixel dimensions	10µm x 10µm
Active area 10µm x	5.1 / 10.2 / 20.5
Active pixels per line	512 / 1024 / 2048
Isolation pixels per line	14

Table 1. IL-P1-xxxx-B Pin Functional Description

Pin	Symbol	Name
1,13	VLOW	Low Bias Voltage
2,18	VDD	Amplifier Supply Voltage
3	OS1	Output Signal 1
4	VSET	Output Node Set Gate Voltage
5	CRLAST	Readout Clock, Last storage phase
6, 22	CR1S	Readout Clock, Phase 1—Storage Phase
7, 23	CR2S	Readout Clock, Phase 2—Storage Phase
8	TCK	Transfer Clock
9	PR	Pixel Reset Clock
10	VPR	Pixel Reset Drain Voltage
11, 28	CR1B	Readout Clock, Phase 1—Barrier Phase
12, 27	CR2B	Readout Clock, Phase 2—Barrier Phase
14, 15, 17, 19	VHIGH	High Bias Voltage
16	NC	No Connection
20, 21, 26	VBB	Substrate Bias Voltage
24	VSTOR	Storage Well Voltage
25, 29	VSS	Ground Reference
30	OS2	Output Signal 2
31	VOD	Output Reset Drain Voltage
32	RST	Output Reset Clock

VLOW	1	32	RST
VDD	2	31	VOD
OS1	3	30	OS2
VSET	4	29	VSS
CRLAST	5	28	CR1B
CR1S	6	27	CR2B
CR2S	7	26	VBB
TCK	8	25	VSS
PR	9	24	VSTOR
VPR	10	23	CR2S
CR1B	11	22	CR1S
CR2B	12	21	VBB
VLOW	13	20	VBB
VHIGH	14	19	VHIGH
VHIGH	15	18	VDD
NC	16	17	VHIGH
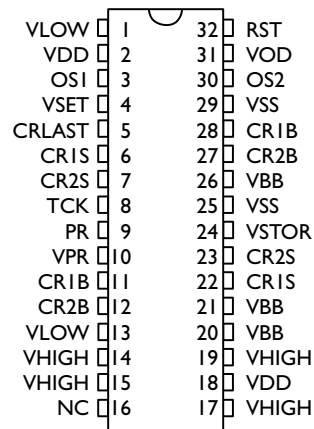
Figure 1. IL-P1-xxxx-B Block Diagram
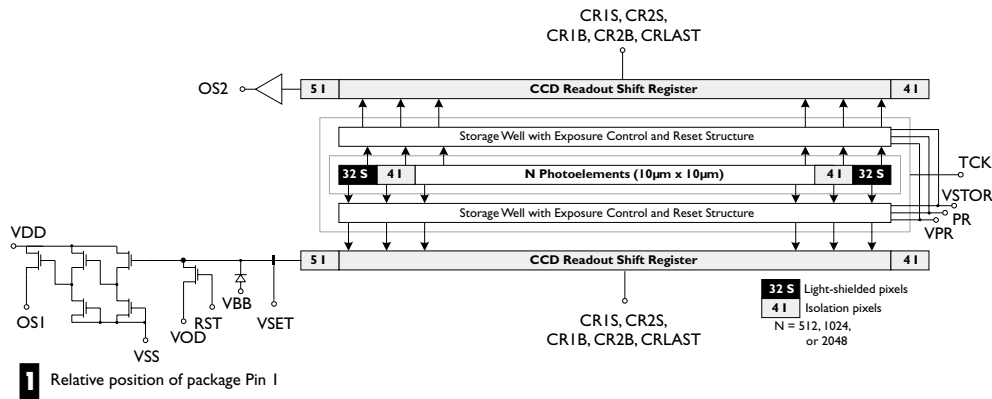
Table 2. # of Clock Drivers Required

Clock Drivers		Min. # Required [1]	
Voltage	Speed	PR [2] off	PR on
Low	High	3	3
High	Low	1	2

1. Redundant clock drivers may be required to drive the CCD input capacitance. Refer to Figure 7 for details.
2. PR = Pixel Reset (exposure control).

Table 3. # of DC Biases Required

DC Biases	# Required [1]	
Regulated?	PR [2] off	PR on
Yes	10	9
No	3	3

1. Refer to Figure 7 for details.
2. PR = Pixel Reset (exposure control).

Shielded pixels per line	32

DALSA's IL-P1-xxxx-B series of linear CCD image sensors use proprietary technology to provide two outputs at 25 MHz each. The series employs buried channel CCD shift registers to maximize output speed and reduce noise. The sensor has a dynamic range of >3200:1 and provides output which is linear for the operating range of light input. The IL-P1-xxxx-B's exposure control allows integration times shorter than the readout time. Proprietary DALSA image sensor architecture provides low image lag pixels and high blue response.

The IL-P1-xxxx-B sensor's superior performance makes it ideally suited for applications requiring maximum speed and high resolution, such as:

- High performance document scanning
- Inspection
- Optical character recognition

Functional Description

The IL-P1-xxxx-B sensor is composed of three main functional groups: photodiodes in which the signal charge packets are generated, two CCD readout shift registers, and two output amplifiers where the charge packets are converted to voltage pulses.

Detection

The IL-P1-xxxx-B series includes sensors with 512, 1024, or 2048 pixels with active imaging area lengths of 5, 10, and 20mm respectively. Photoelements are 10µm square for a photosensitive area of $100µm^2$ and a 1:1 aspect ratio. Light incident on these photoelements is converted into charge packets whose size (i.e., number of electrons) is linearly dependent on the light intensity and the integration time. The charge is collected into a separate storage well (VSTOR) adjacent to each photoelement. This helps to minimize both image lag and nonuniformities associated with the use of pixel reset.

 With exposure control disabled, integration time is the period between successive pulses of the transfer (TCK) clock. Integration time can be further reduced with electronic exposure control using the pixel reset (PR) clock. The pixel reset clock resets not the photoelements themselves but the storage well adjacent to each photoelement. When PR is clocked, the integration time becomes the duration between the falling edge of the PR clock and the rising edge of the TCK clock.

When PR is clocked, the PR pulse must be damped to produce a smooth PR pulse. If PR switches too rapidly, the uniformity of the OSn signals will be affected by the PR clock feedthrough.

Antiblooming is always present when biases fall within the specified operating conditions. By adjusting VSTOR however, the user has the added flexibility of selecting the antiblooming level (the signal level beyond which additional signal charges are drained away). A higher VSTOR bias results in a higher antiblooming level.

Transfer

The TCK clock controls the transfer of electrons from the storage well into two discrete readout registers for alternating odd/even pixel readout. Transfer is from the storage wells into the CR1 phases of the readout registers. The readout registers are then used to serially shift the charge packets to the two high-speed low-noise output amplifiers.

The two readout registers are pseudo-2-phase buried-channel CCD shift registers. The CR1x and CR2x phases are complements of each other. Each of these two phases has a storage (CRxS) and a barrier (CRxB) gate. The storage and barrier gates of each phase are clocked in phase (i.e., CR1S is clocked in phase with CR1B, and CR2S is clocked in phase with CR2B). The only difference between the storage and barrier phase clocks is the bias levels applied to these clocks. AC-coupling and then DC-shifting the CRxS phases will produce the CRxB phases.

The final storage electrode of each readout register is connected separately to CRLAST. CRLAST should be clocked in phase with CR1.

All CR clocks operate with 50% duty cycle.

Unlike CR1 and CR2, the CRLAST pin is connected to only two CCD gates, one for each of the two CCD shift registers on each side. Consequently, the CRLAST capacitance is much smaller than the CR1 or CR2 capacitance. To prevent CRLAST from switching much faster than CR1 and CR2, we recommend that a 100Ω resistor be connected in series with CRLAST. The CRLAST clock

should preferably have a slower rise and fall time than CR1 and CR2.

Additional details on driving the sensor are provided on Figure 7.

Output

The signal charge packets from the readout shift registers are transferred serially from the last readout gate (CRLAST), over the set gate (VSET), to a floating sense node diffusion. The set gate isolates the sense node diffusion from the last readout gate and the rest of the readout shift register. As signal charge accumulates on the floating node diffusion, the potential of this diffusion decreases. The floating node diffusion is connected to the input of a 2.5-stage low-noise amplifier, producing an output signal voltage on the amplifier output (OSn). The floating diffusion is cleared of signal charge by the reset gate (RST) in preparation for the next signal charge packet. The voltage level of the floating diffusion after each reset is determined by the output reset drain voltage (VOD). AC coupling the output is recommended to eliminate the DC offset.

Each of the output signals (OSn) requires an off-chip load drawing approximately 8mA of load current. If the sensor is running at greater than 35MHz data rate, or if the load capacitance (C_{LOAD}) is greater than 10pF, larger load current (up to the 18mA limit) may be required. As the load current increases, the amplifier bandwidth increases. The amplifier can also drive larger capacitive loads when the load current is larger. We recommend however that just enough bandwidth be used since larger bandwidth also results in increased noise.

If an off-chip current load is not available, each of the amplifier outputs (OSn) can be connected to a 1.2kΩ load resistor. The use of a passive (resistive) load reduces the amplifier gain, resulting in lower responsivity and saturation output signal.

The variations in charge conversion efficiency among the various outputs of the sensor, along with component variations in the drive electronics, result in output gain mismatch. To match outputs, we recommend that the camera electronics incorporate a gain correction of up to 15%.

Table 4. IL-P1-xxxx-B Absolute Maximum Ratings

Parameter	Unit	Min.	Max.
Storage Temp	°C	-20	80
Operating Temp	°C	-20	60
Voltage on CR1x, CR2x, CRLAST, RST, VSET, VSTOR, TCK, PR with respect to VBB	V	-10	18
Voltage on OSn, VDD, VOD, VSS, VPR, VHIGH, VLOW with respect to VBB	V	0	18
Voltage on OSn with respect to VSS	V	VDD-8	VDD+1
Amplifier Load Current (I_{LOAD})	mA per output		20

WARNING: Exceeding these values will void product warranty and may damage the device.

CAUTION! These devices are sensitive to damage from electrostatic discharge (ESD). The leads should be shorted together during storage or handling to prevent damage to the device.

Table 5. IL-P1-xxxx-B Input/Output Characteristics

Input Characteristics: Capacitance to VBB [1]	Unit	Typical		
		512	1024	2048
from CR1S, CR2S[1]	pF	90	130	220
from CR1B, CR2B[2]	pF	100	140	240
from CRLAST	pF	12	12	12
from RST	pF	10	10	10
from PR	pF	40	60	110
from TCK	pF	70	110	200
Output Characteristics:				
Output Impedance (R_{OUT})[4]	Ω	180Ω with I_{LOAD} = 8mA		
Amplifier Supply Current (I_{DD}) [5]	mA	36mA with I_{LOAD} = 8mA		
DC Output Offset (VOS) [6]	V	10V with I_{LOAD} = 8mA		

Notes:

1. Using 1V pk-pk 1MHz signal with +5V DC offset.
2. The two CR1S pins (pins 6 and 22) are internally connected, as are the two CR2S pins (pins 7 and 23).
3. The two CR1B pins (pins 11 and 28) are not internally connected, nor are the two CR2B pins (pins 12 and 27). Capacitance values indicated refer to the total capacitance of the two CRxB pins.
4. In general, R_{OUT} (Ω) $\simeq$ 520 * $(I_{LOAD})^{-0.5}$, I_{LOAD} in mA.
5. In general, I_{DD} (mA) = 2 * (10 + I_{LOAD}), I_{LOAD} in mA.
6. In general, V_{OFFSET} (V) = 0.003 * $(I_{LOAD})^2$ - 0.22 * (I_{LOAD}) + 11.5, I_{LOAD} in mA.

Table 6. IL-P1-xxxx-B DC Operating Conditions

Symbol	Description	Unit	Min.	Rec. [1]	Max.
I_{LOAD} [2]	Load current to each output (OSn)	mA	7.5	8.0	18.0
VDD	Amplifier supply voltage	V	14.0	14.0	15.0
VOD	Output reset drain voltage	V	11.0	11.3	VDD - 2
VSET	Output node set gate voltage	V	CRLAST offset +0.5	0	CRLAST offset +1.0
VSTOR [3]	Storage well voltage	V	-1	0	0.2
VPR	Pixel reset drain voltage	V	13	14	15
VBB	Substrate bias	V	-3	-2	-1
VLOW [4]	Low bias voltage	V	VBB	0	0
VHIGH	High bias voltage	V	13	14	15
VSS	Ground Reference	V		0	

Notes:

1. Selecting a bias that deviates significantly from the recommended value can cause the recommended value of another bias to fall outside the Min. and Max. bias range. If this occurs, ignore the recommended value and ensure that each of the biases falls within its own Min. and Max. range.

2. I_{LOAD} needs to be > 10mA only if f_{RST} > 35MHz or C_{LOAD} > 10pF.

3. VSTOR may be adjusted to affect the antiblooming level. V_{SAT} decreases by ~418mV for every 1.0V reduction in VSTOR.

4. If your implementation uses separate digital and analog grounds, connect VLOW to the digital ground.

Table 7. IL-P1-xxxx-B AC Operating Conditions

Symbol	Description		Unit	Min.	Rec.	Max.
CRx	All CR Clocks	swing*	V	4.5	5.0	6.5
CRxS	Readout Register Clocks (storage phase)	offset*	V	0	0	0.5
CRxB	Readout Register Clocks (barrier phase)	offset	V	-(CRx swing)+1.5	-3.0	-(CRx swing)+2.5
CRLAST	Readout Register Clocks (last storage phase)	offset	V	CRxB offset+1.5	-0.8	CRxB offset+2.5
RST	Reset Clock	offset	V	VOD-RST swing-6.8	-0.5	0
		swing	V	4.8	5.5	6.5
TCK	Transfer Clock	offset	V	VBB	0	0
		swing	V	VSTOR+5.0	8	10
PR	Pixel Reset Clock	offset	V	0.5	1.2	1.5
		swing	V	VSTOR+4.5	8	10
f_{RST}	Data rate per output		MHz		25	40
f_{DATA}	Effective data rate		MHz		50	80
f_{LINE}	Line rate	0512	kHz		87.3	137.5
		1024			46.1	73.1
		2048			23.7	37.8

Notes:

1. Selecting a bias that deviates significantly from the recommended value can cause the recommended value of another bias to fall outside the Min. and Max. bias range. If this occurs, ignore the recommended value and ensure that each of the biases falls within its own Min. and Max. range.
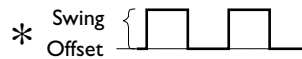
✱ Swing
Offset

Table 8. IL-P1-xxxx-B Performance Specifications

Specification		Unit	Min.	Typ.	Max.
Saturation Output Voltage (VSAT)		mV	700	900	1100
rms Noise		mV		0.28	0.31
Wavelength of Peak Responsivity		nm		700	
Peak Responsivity		V/(μJ/cm^2)	11.0	12.0	13.5
Dynamic Range			2250:1	3200:1	3900:1
Charge Conversion Efficiency (CCE)		μV/e$^-$	4.7	5.0	5.3
Noise Equivalent Exposure (NEE)		pJ/cm^2	21	23	28
Saturation Equivalent Exposure (SEE)		nJ/cm^2	52	75	
Full Well Capacity		ke$^-$	132	180	
Fixed Pattern Noise (FPN) [1,2]	PR exposure control disabled	mV		0.5	1.0
	PR exposure control enabled	mV		2.0	5.0
Photoresponse Non-Uniformity (PRNU) [3,4]		% OS			
PR exposure control disabled	8 pixel local neighborhood			2.2	6.0
	Global			3.5	8.5
PR exposure control enabled	8 pixel local neighborhood			2.5	6.5
	Global			3.8	8.8
Charge Transfer Efficiency (CTE) (readout register)			0.99999	0.999999	
First Field Lag [5]		mV		11.5	
Dark Signal, Integration time = 84μs		mV		0.15	0.5

Notes:

1. Maximum peak-to-peak variation of all outputs.
2. Due to its general purpose design, DALSA's camera and sensor evaluation hardware provides an output that cannot be used to directly measure low FPN.
3. The peak-to-peak variation is measured at ~50% SEE.
4. With output gain mismatch correction.
5. Lag is measured at VSAT with f_{LINE} = 10kHz.

Test Conditions:

- Operating temperature = 35°C.
- f_{RST} = data rate per output = 25MHz.
- I_{LOAD} = 8mA.
- C_{LOAD} = 10pF.
- Tungsten halogen light source, black body color temperature 3200K, filtered with 750nm IR cutoff filter.
- See Sensor Measurement Definitions (doc# 03-36-00149) for specification definitions.

Figure 2. Performance Measurements

Responsivity

Output vs. Integration Time (@700nm)
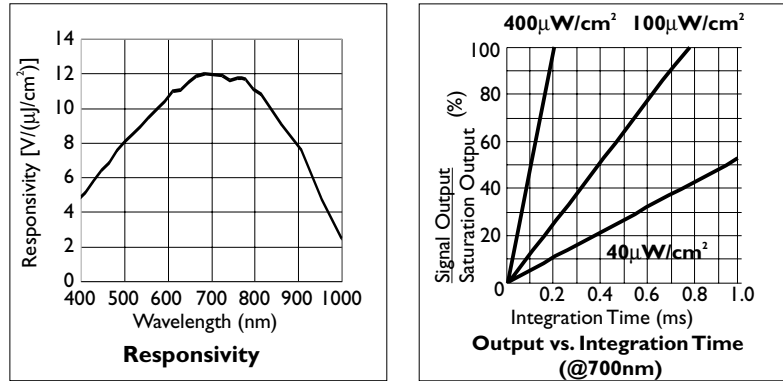
Table 9. IL-P1-xxxx-B Timing Parameters

Symbol	Description	Unit	Min.	Rec.	Max.
t_{CR}	Period of CRx clocks				
t_1	Integration time (PR disabled)				
t_2	Integration time (PR enabled)				
t_3	TCK to first valid pixel	pixels	23		23
t_4	Overclock pixels	pixels	0	23	
t_5	CRxB falling edge to CRxS falling edge	ns	0	0	$0.25t_{CR}$
t_6	CR1B falling edge to CRLAST falling edge	ns	0	0	$0.25t_{CR}$
t_7	TCK high overlap with CR1S high	ns	200	300	
t_8	TCK falling edge to CR1S falling edge	ns	2		
t_9	CRLAST rising to RST rising edge	ns	0	$0.5t_{CR} - t_{11}$	$0.5t_{CR} - t_{11}$
t_{10}	RST falling edge to CRLAST falling edge	ns	0	0	$0.5t_{CR}-t_{11}$
t_{11}	RST pulse width (FWHM)[1]	ns	5	5	$0.25t_{CR}$
t_{12}	CR1x and CR2x rise and fall time	ns	2	5	$0.25t_{CR}$
t_{13}	CRLAST rise and fall time	ns	t_{12}	t_{12} + 1	$0.25t_{CR}$

Notes:

1.   Full Width Half Maximum
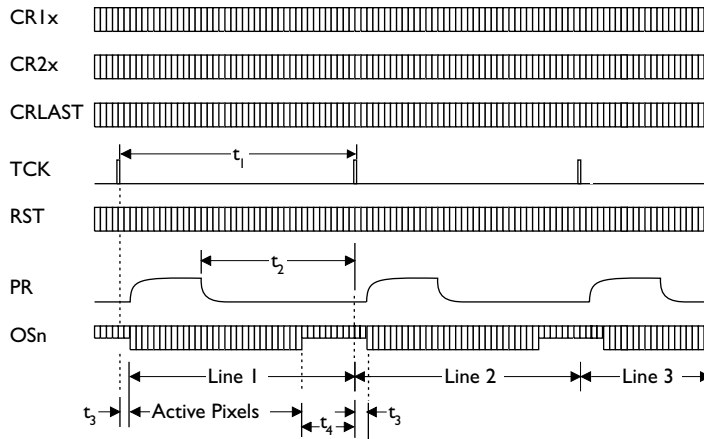
Figure 3. IL-P1-xxxx-B Overall Timing

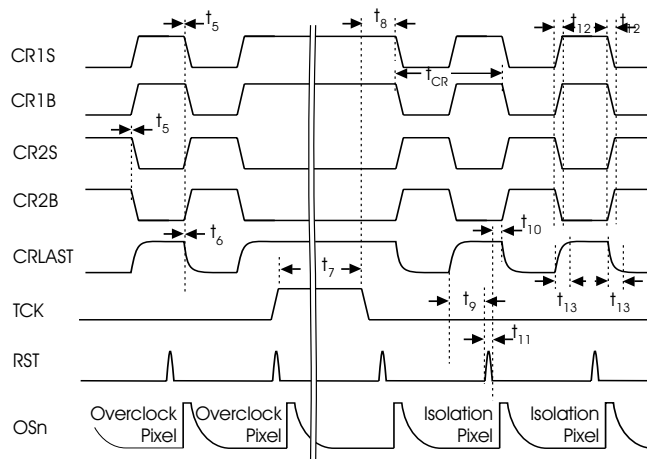## Figure 4. IL-P1-xxxx-B Detailed Readout Register Timing

Figure 5. IL-P1-xxxx-B Gate Structure Diagram

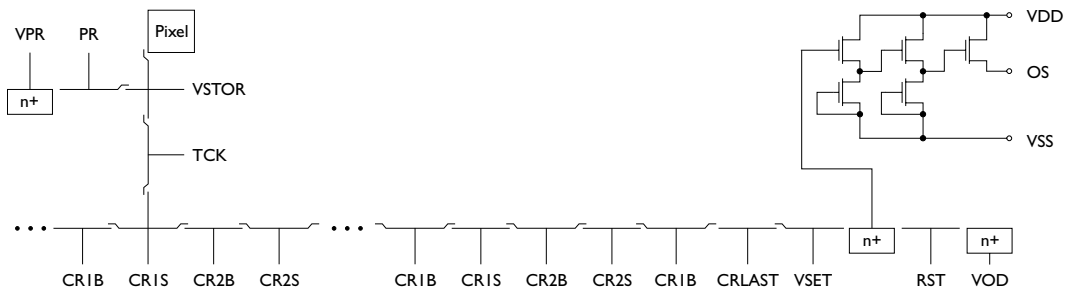For product information and updates visit www.dalsa.com

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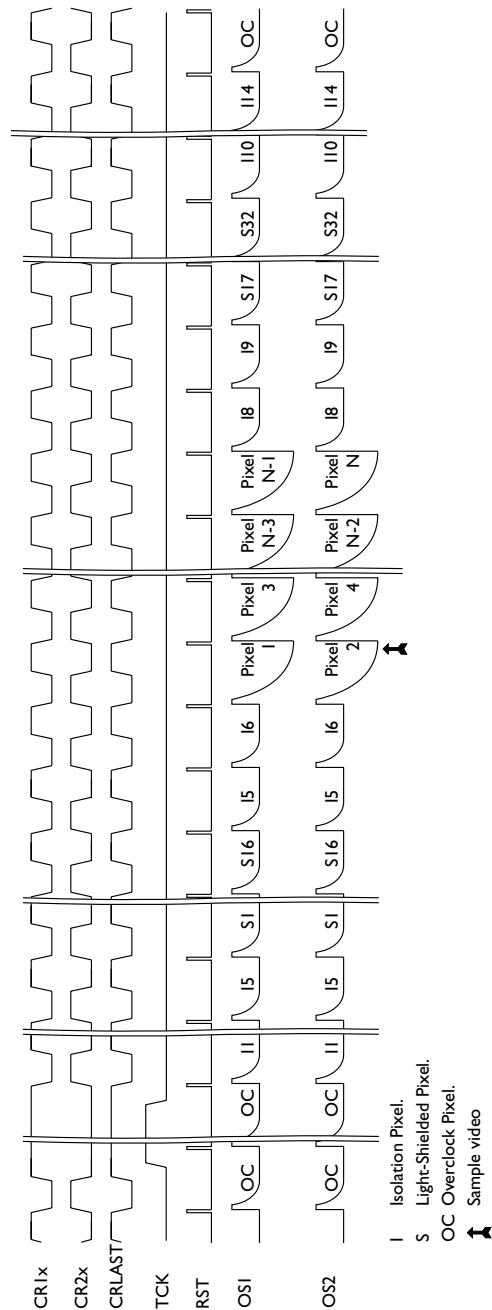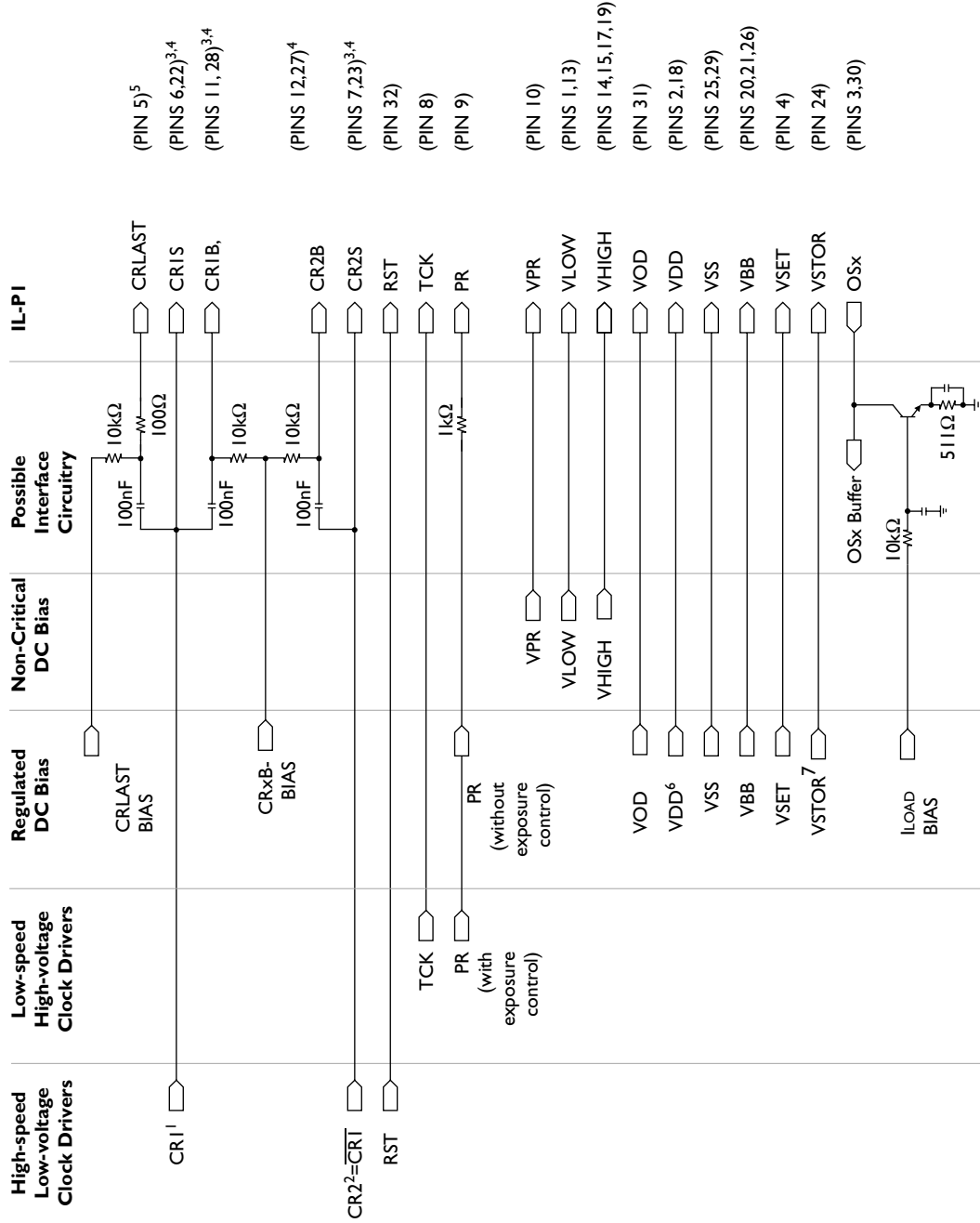## Figure 6. IL-P1-xxxx-B Readout Register Timing

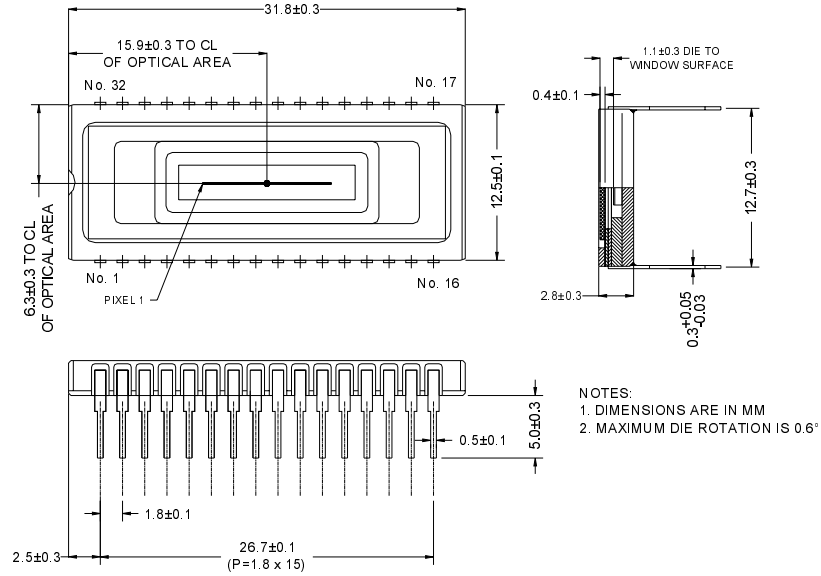# Figure 7. IL-P1-xxxx-B Sensor Operation Connections

Notes to Figure 7.

1. Clock drivers are designed to drive only up to a maximum capacitance (C_{MAX}) at a given clock frequency. If the total capacitances of CRLAST, CR1S, and CR1B (see Table 5) exceed C_{MAX}, more than one CR1 driver is required.

2. Clock drivers are designed to drive only up to a maximum capacitance (C_{MAX}) at a given clock frequency. If the total capacitances of CR2S and CR2B (see Table 5) exceed C_{MAX}, more than one CR2 driver is required.

3. Both pins should be connected to clock drivers, though not necessarily to the same clock driver. If more than one clock driver is used, it is acceptable to drive each pin from separate drivers.

4. Although the sensors are sufficiently robust that the rise and fall times of CRxS and CRxB do not need to be very closely matched, performance is more optimal if attempts are made to match the CRxS and CRxB rise and fall times. If more than one CRx clock driver is used, time constants are more closely matched if the sensor is driven using either one of the following configurations:

a. Drive the CRxS pins with n CRx drivers. Tie the CRxB pins together. Drive the CRxB pins with a separate set of n CRx drivers.

b. Drive the CRxS pins with 2n CRx drivers. Drive each CRxB pin separately with separate sets of n CRx drivers.

c. Connect a 10Ω resistor in series with CRxS. Drive the CRxS pins with n CRx clock drivers. Connect a 20Ω resistor in series with each CRxB pin. Drive each CRxB pin with separate sets of n CRx drivers.
   Note that the CRxS pins are internally connected together, while the CRxB pins are not.

5. CRLAST should not have a fall time that is much faster than the fall time of CR1B. Unlike CR1B however, the CRLAST pin is connected to only two CCD gates, one for each of the CCD shift registers. Consequently, the CRLAST capacitance is much smaller than the CR2B capacitance. This is not an issue if the CRLAST clock is tapped from CR1. However, if CRLAST is being driven from a separate driver, we recommend that a 150Ω resistor be connected in series with CRLAST.

6. Need to source $I_{DD} = 2 * (10 + I_{LOAD})$ mA.

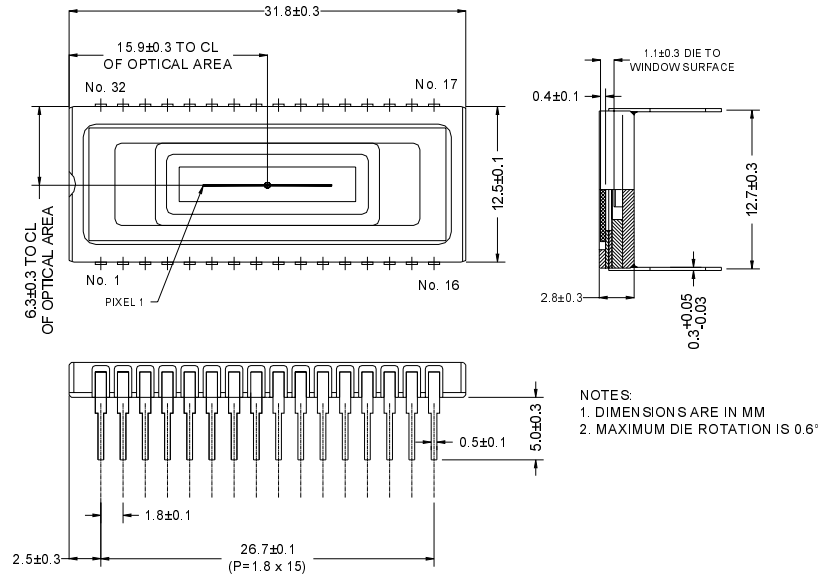7. May have an optional antiblooming level adjustment.

ISO 9001 DALSA maintains a registered quality system meeting the ISO 9001 standard.

Figure 8. IL-P1-xxxx-B Package Dimensions

0512

1024

2048

31.8±0.3

15.9±0.3 TO CL
OF OPTICAL AREA

No. 32

No. 17

12.5±0.1

6.3±0.3 TO CL
OF OPTICAL AREA

No. 1

No. 16

PIXEL 1

1.1±0.3 DIE TO
WINDOW SURFACE

0.4±0.1

12.7±0.3

2.8±0.3

0.3$^{+0.05}_{-0.03}$

5.0±0.3

0.5±0.1

NOTES:
1. DIMENSIONS ARE IN MM
2. MAXIMUM DIE ROTATION IS 0.6°

1.8±0.1

2.5±0.3

26.7±0.1
(P=1.8 x 15)